1. In a silicon based semiconductor transistor device which includes a gate, a source region, a drain region, and a channel region coupling the source region and drain region, the improvement comprising:

a dynamically adjustable threshold voltage associated with the silicon based semiconductor transistor device, and which threshold voltage is controlled at least in part using a bias voltage applied across the gate and source region of the semiconductor transistor device.

2. The silicon based semiconductor transistor device of claim 1, further wherein said gate and source region are located on a silicon on insulator substrate.

3. The silicon based semiconductor transistor device of claim 1, wherein said dynamically adjustable threshold voltage is caused by a trapping and detrapping mechanism associated with charge carriers in a channel region of the silicon based semiconductor transistor device.

4. The silicon based semiconductor transistor device of claim 1, wherein said dynamically adjustable threshold voltage can be altered while the device is turned on.

5. In a silicon based semiconductor transistor device which includes a gate, a source region, a drain region, and a channel region coupling the source region and drain region, the improvement comprising:

a threshold voltage associated with the silicon based semiconductor transistor device which is dynamically adjustable and related to a bias voltage applied across the gate and source region of the semiconductor transistor device;

wherein said threshold voltage can be adjusted during operation of the silicon based semiconductor device using said bias voltage.

6. The silicon based semiconductor transistor device of claim 5, wherein said threshold voltage can be adjusted up or down.

7. The silicon based semiconductor transistor device of claim 6, wherein a first time required to adjust said threshold voltage up is approximately equal to a second time required to adjust said threshold voltage down.

8. A silicon based semiconductor field effect transistor (FET) which includes a gate, a source region, a drain region, and a channel region coupling the source region and drain region and comprising:

a channel conduction control region, which channel conduction control region is part of the FET gate and is adapted to generate a first electric field which controls a density of electrons available for conduction in the channel region of the FET;

wherein said first electric field operates to counter a movement of carriers into the channel region caused by a separate second electric field associated with a gate bias voltage applied to the FET;

and further wherein said threshold voltage can be dynamically adjusted during operation of the silicon based semiconductor device using said gate bias voltage.

9. The FET of claim 8, wherein said first electric field generated by said channel conduction control region is controlled in part by said gate bias voltage.

10. The FET of claim 8 wherein said first electric field generated by said channel conduction control region is controlled in part by a drain bias voltage.

11. The FET of claim 8, wherein said channel conduction control region is doped with an impurity type which is the same as a substrate region of the FET, and opposite to an impurity type used in said source region and said drain region.

12. A silicon based semiconductor field effect transistor (FET) which includes a gate, a source region containing a first dopant of a first conductivity type, a drain region also containing said first conductivity type dopant, and a channel region coupling the source region and drain region, comprising:

a channel conduction control region, which channel conduction control region is part of the gate and contains a second dopant opposite said first conductivity type, said channel conduction control region being responsive to a gate bias voltage applied to the FET, and operating to generate a first electric field which controls a density of electrons available for conduction in the channel region of the FET;

wherein said first electric field operates to counter conduction in the channel caused by a separate electric field resulting from the gate bias voltage applied to the FET;

wherein a threshold voltage of the FET can be dynamically adjusted during operation of the silicon based semiconductor device using said gate bias voltage.

13. The FET of claim 12, wherein said FET can be operated with a negative differential resistance mode.

14. In a silicon based semiconductor transistor device which includes a gate, a source region, a drain region, and a channel region coupling the source region and drain region, the improvement comprising:

a dynamically adjustable threshold voltage associated with the silicon based semiconductor transistor device, and which threshold voltage is adjusted at least in part under control of a bias voltage applied across the source region and drain region of the semiconductor transistor device.

15. The silicon based semiconductor transistor device of claim 14, wherein said bias voltage can be used to turn off said device independently of a gate bias voltage.

16. The silicon based semiconductor transistor device of claim 14, wherein said device can be operated with a negative differential resistance mode.

17. In a silicon based semiconductor transistor device which includes a gate, a source region, a drain region, and a channel region coupling the source region and drain region, the improvement comprising:

a dynamically adjustable threshold voltage associated with the silicon based semiconductor transistor device, and which threshold voltage is adjusted using a first bias voltage applied across the source region and drain region of the silicon based semiconductor transistor device, and a second bias voltage applied across the source region and gate of the silicon based semiconductor transistor.

18. The silicon based semiconductor transistor device of claim 17, wherein said device can be operated with a negative differential resistance (NDR) mode in response to a separate NDR bias signal applied to the device.

19. The silicon based semiconductor transistor device of claim 17, wherein said device is formed as part of a memory circuit.

20. The silicon based semiconductor transistor device of claim 17, wherein said dynamically adjustable threshold voltage can be adjusted up or down at approximately the same rate.